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		Application Number	10/635,942		
TRANSMITTAL FORM			Filing Date	August 7, 2003	
			First Named Inventor	Tom RICHARDSON	
(to be used for all	l correspondence afte	r initial filing)	Group Art Unit	2184	
			Examiner Name	Not yet assigned	
Total Number of	Pages in This Submi	ssion 1	Attorney Docket Number	Flarion-75APP (101)	
		ENCL	OSURES (check a	all that apply)	
Fee Transmittal Form Fee Attached Drawing Amendment / Reply After Final Petition Provision Extension of Time Request Express Abandonment Request Request Request		to Convert to a mail Application of Attorney, Revocation of Correspondence	After Allowance Communication to Group Appeal Communication to Board of Appeals and Interferences Appeal Communication to Group (Appeal Notice, Brief, Reply Brief) Proprietary Information Status Letter Postcard Receipt Other Enclosure(s) (please identify below): References DA-DM		
	SIGNATU	JRE OF APPLI	CANT, ATTORNEY, OR A	GENT	
Firm or Individual name Signature Michael P. Straub					
Date January 18, 2005		,	value	- · · · · · · · · · · · · · · · · · · ·	
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No.: Flarion-75APP (101)

Applicant: Tom RICHARDSON et al.

Serial No.: 10/635,942

Filing Date: August 7, 2003

Title: SOFT INFORMATION SCALING FOR ITERATIVE DECODING

Examiner: Not yet assigned

Group Art Unit: 2184

Mail Stop Patent Application Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

SIR:

Information Disclosure Statement Transmittal

The applicants respectfully request that the references listed on the attached PTO/SB/08A be considered in the examination of the above-identified application A copy of each of these references, except for U.S. patents and patent application publications is enclosed. (See the notice, "Information Disclosure Statements May Be Filed Without Copies of U.S. Patents and Published Applications in Patent Applications Filed After June 30, 2003," Pre-OG Notices (July 11, 2003).)

The applicants reserve the right to establish that any of the references listed on the attached PTO/SB/08A are not prior art to the above-captioned application.

Since a first Office Action on the merits has not yet been received, the applicants assume that this Information Disclosure Statement should be considered under 37 C.F.R. §§ 1.97(b)(3). Accordingly, it is believed that no fee is due. If, however, an Office Action on the merits has been mailed before the filing date of this Information Disclosure Statement, the Office is authorized to charge any fee required to have the Information Disclosure Statement considered to the deposit account of Straub & Pokotylo, deposit account number 50-1049.

Respectfully submitted,

Dated: January 18, 2005

Michael P. Straub, Attorney

Reg. No. 36,941 Customer No. 26479 (732) 542-9070

STRAUB & POKOTYLO 620 Tinton Avenue Bldg. B, 2nd Floor Tinton Falls, NJ 07724-3260

CERTIFICATE OF MAILING under 37 C.F.R. 1.8(a)

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Attorney Docket No.:

of

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Flarion-75APP (101)

			U.S. PATEN	T DOCUMENTS	
Examiner Initials*	Cite No.1	U.S. Patent Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	. Pages, Columns, Lines where relevant Passages or Figures appear
	BA	3,542,756	Nov 24 1970	Gallager	
	BB	3,665,396	May 23 1972	Forney, Jr	
	BC	4,295,218	Oct 13 1981	Tanner	
	BD	5,157,671	October 20, 1992	Karplus	
	BE	5,293,489	March 8, 1994	Furui et al	
	BF	5,313,609	May 17, 1994	Baylor et al	
	BG	5,396,518	Mar 7 1995	How	
	BH	5,457,704	Oct 10 1995	Hoeher et al	
	BI	5,526,501	June 11 1996	Shams	
	BJ	5,860,085	Jan 12 1999	Storman	
	BK	5,864,703	January 26, 1999	van Hook et al.	
	BL	5,892,962	Apr 6 1999	Cloutier	
	BM	5,933,650	August 3, 1999	van Hook et al.	
	BN	5,968,198	Oct 19 1999	Hassan	
	ВО	6,002,881	December 14, 1999	York et al.	
	BP	6,073,250	June 6, 2000	Luby et al.	
	BQ	6,195,777	Feb 27 2001	Luby et al	
	BR	6,247,158	June 12 2001	Smallcomb	
	BS	6,266,758	July 24, 2001	van Hook et al.	
	BT	6,298,438	October 2, 2001	Thayer et al	
	BU	6,339,834	Jan 15 2002	Crozier et al.	
	BV	6,397,240	May 28, 2002	Fernando et al.	
	BW	6,438,180	Aug 20 2002	Kavcic et al	
	BX	6,473,010	Oct 29 2002	Viyaev et al.	
	BY	6,526,538	February 25, 2003	Hewitt	
	BZ	6,633,856	October 14, 2003	Richardson et al	
********	CA	US2004/0034828	February 19, 2004	Hocevar	
	CB	6,718,504	April 6, 2004	Coombs et al	
	CC	6,731,700	May 4 2004	Yakhnich et al	
	CD	6,754,804	June 22, 2004	Hudepohl et al	

Examiner Initials*	Cite No.1	Foreign Patent Document Office ³ Number ⁴	MM-DD-YYYY Document		Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	Т6

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¹ Unique citation designation number. 2 See attached kinds of U.S. Patent Documents. 3 Enter Office that Issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the Indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5 Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16, if possible. 6 Applicant is to place a check mark here if English language translation is attached.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Complete if Known

10/635,942

Application Numbers Filing Date ADEM August 7, 2003 Tom RICHARDSON First Named Inventor:

Group Art Unit:

2184

Not yet assigned

Examiner Name: 2 2 Flarion-75APP (101) Sheet of Attorney Docket No.:

Examiner Cite Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, includes and include		OTHER REFERENCES - NON-PATENT LITERATURE DOCUMENTS					
DA Richardson et al. The capacity of low-density parity-check codes under message-passing Decoding, IEEE Transactions on Information Theory; pages: 599-618, February 2001, (same inventor) whole document. DB Paranchych et al. Performance of a digital symbol synchronizer in cochannel interference and noise, IEEE Transactions on Communications, pages: 1945-1954; Nov. 2000, whole document. DC NN77112415. Digital Encoding of Wide Range Dynamic Analog Signals, IBM Tech. Disclosure Bulletin, November 1, 1997, VOL. No. 20; ISSUE No. 6; Pages 2415-2417, whole document DD NN9210335. Hierarchical Coded Modulation of Data with Fast Decaying Probability Distributions, IBM Tech. Disclosure Bulletin, October 1992, VOL. No. 35; ISSUE No. 5; Pages 335-336, whole document. DE Sorokine, V. et al. Innovative coding scheme for spread-spectrum communications, The Ninth IEEE International Symposium on Indoor and Mobile Radio Communications, pages: 1491-1495, Vol. 3; September 1998, whole document. DF T. Moors and M. Verearaghavan, "Preliminary specification and explanation of Zing: An end-to-end protocol for transporting bulk data over optical circuits", pp. 1-55 (May 2001). DG T. Richardson and R. Urbanke, "The Capacity of Low-Density Parity-Check Codes under Message-Passing Decoding", pp. 1-44 (March 2001). DH T. Richardson and R. Urbanke, "An Introduction to the Analysis of Iterative Coding Systems", pp. 1-36. DJ Saied Hemati, Amir H. Banihashemi, VLSI circuits: Iterative decoding in analog CMOS, Proceedings of the 13th ACM Great Lakes Symposium on VLSI April 2003, Pages:15-20. DK Mohammad M. Mansour, Naresh R. Shanbhag, Session 11: Low-power VLSI decoder architectures for LDPC codes, Proceedings of the 2002 international symposium on Low power electronics and design August 2002, Pages: 284-289. DL R. Blahut, "Theory and Practice of Error Control Codes", Library of Congress Cataloging in Publication Data, pp-47-49, (May 1984) DM W. W. Peterson and E.J. Weldon, Jr., "Error-Correcting Codes", Second Edition, The	1		Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume, issue number(s), publisher, country, where published, source	T ²			
Decoding, IEEE Transactions on Information Theory; pages: 599-618, February 2001, (same inventor) whole document. DB Paranchych et al. Performance of a digital symbol synchronizer in cochannel interference and noise, IEEE Transactions on Communications, pages: 1945-1954; Nov. 2000, whole document. DC NN77112415. Digital Encoding of Wide Range Dynamic Analog Signals, IBM Tech. Disclosure Bulletin, November 1, 1997, VOL. No. 20; ISSUE No. 6; Pages 2415-2417, whole document DD NN9210335. Hierarchical Coded Modulation of Data with Fast Decaying Probability Distributions, IBM Tech. Disclosure Bulletin, October 1992, VOL. No. 35; ISSUE No. 5; Pages 335-336, whole document. DE Sorokine, V. et al. Innovative coding scheme for spread-spectrum communications, The Ninth IEEE International Symposium on Indoor and Mobile Radio Communications, pages: 1491-1495, Vol. 3; September 1998, whole document. DF T. Moors and M. Veeraraghavan, "Preliminary specification and explanation of Zing: An end-to-end protocol for transporting bulk data over optical circuits", pp. 1-55 (May 2001). DG T. Richardson and R. Urbanke, "The Capacity of Low-Density Parity-Check Codes under Message-Passing Decoding", pp. 1-44 (March 2001). DH T. Richardson, A. Shokrollahi, R. Urbanke, "Design of Capacity-Approaching Irregular Low-Density Parity-Check Codes", pp. 1-43 (March 2001). DI T. Richardson and R. Urbanke, "An Introduction to the Analysis of Iterative Coding Systems", pp. 1-36. DJ Saied Hemati, Amir H. Banihashemi, VLSI circuits: Iterative decoding in analog CMOS, Proceedings of the 13 th ACM Great Lakes Symposium on VLSI April 2003, Pages:15-20. DK Mohammad M. Mansour, Naresh R. Shanbhag, Session 11: Low-power VLSI decoder architectures for LDPC codes, Proceedings of the 2002 international symposium on Low power electronics and design August 2002, Pages: 284-289. DL R. Blahut, "Theory and Practice of Error Control Codes", Library of Congress Cataloging in Publication Data, pp-47-49, (May 1984) DM W. W. Peterson and E.J. Weldon, Jr.							
DB Paranchych et al. Performance of a digital symbol synchronizer in cochannel interference and noise, IEEE Transactions on Communications, pages: 1945-1954; Nov. 2000, whole document. DC NN77112415. Digital Encoding of Wide Range Dynamic Analog Signals, IBM Tech. Disclosure Bulletin, November 1, 1997, VOL. No. 20; ISSUE No. 6; Pages 2415-2417, whole document DD NN9210335. Hierarchical Coded Modulation of Data with Fast Decaying Probability Distributions, IBM Tech. Disclosure Bulletin, October 1992, VOL. No. 35; ISSUE No. 5; Pages 335-336, whole document. DE Sorokine, V. et al. Innovative coding scheme for spread-spectrum communications, The Ninth IEEE International Symposium on Indoor and Mobile Radio Communications, pages: 1491-1495, Vol. 3; September 1998, whole document. DF T. Moors and M. Veeraraghavan, "Preliminary specification and explanation of Zing: An end-to-end protocol for transporting bulk data over optical circuits", pp. 1-55 (May 2001). DG T. Richardson and R. Urbanke, "The Capacity of Low-Density Parity-Check Codes under Message-Passing Decoding", pp. 1-44 (March 2001). DH T. Richardson, A. Shokrollahi, R. Urbanke, "Design of Capacity-Approaching Irregular Low-Density Parity-Check Codes", pp. 1-43 (March 2001). DI T. Richardson and R. Urbanke, "An Introduction to the Analysis of Iterative Coding Systems", pp. 1-36. DJ Saied Hemati, Amir H. Banihashemi, VLSI circuits: Iterative decoding in analog CMOS, Proceedings of the 13 th ACM Great Lakes Symposium on VLSI April 2003, Pages:15-20. DK Mohammad M. Mansour, Naresh R. Shanbhag, Session 11: Low-power VLSI decoder architectures for LDPC codes, Proceedings of the 2002 international symposium on Low power electronics and design August 2002, Pages: 284-289. DL R. Blahut, "Theory and Practice of Error Control Codes", Library of Congress Cataloging in Publication Data, pp-47-49, (May 1984) DM W. W. Peterson and E.J. Weldon, Jr., "Error-Correcting Codes", Second Edition, The							
and noise, IEEE Transactions on Communications, pages: 1945-1954; Nov. 2000, whole document. DC NN77112415. Digital Encoding of Wide Range Dynamic Analog Signals, IBM Tech. Disclosure Bulletin, November 1, 1997, VOL. No. 20; ISSUE No. 6; Pages 2415-2417, whole document DD NN9210335. Hierarchical Coded Modulation of Data with Fast Decaying Probability Distributions, IBM Tech. Disclosure Bulletin, October 1992, VOL. No. 35; ISSUE No. 5; Pages 335-336, whole document. DE Sorokine, V. et al. Innovative coding scheme for spread-spectrum communications, The Ninth IEEE International Symposium on Indoor and Mobile Radio Communications, pages: 1491-1495, Vol. 3; September 1998, whole document. DF T. Moors and M. Veeraraghavan, "Preliminary specification and explanation of Zing: An end-to-end protocol for transporting bulk data over optical circuits", pp. 1-55 (May 2001). DG T. Richardson and R. Urbanke, "The Capacity of Low-Density Parity-Check Codes under Message-Passing Decoding", pp. 1-44 (March 2001). DH T. Richardson, A. Shokrollahi, R. Urbanke, "Design of Capacity-Approaching Irregular Low-Density Parity-Check Codes", pp. 1-43 (March 2001). DI T. Richardson and R. Urbanke, "An Introduction to the Analysis of Iterative Coding Systems", pp. 1-36. DJ Saied Hemati, Amir H. Banihashemi, VLSI circuits: Iterative decoding in analog CMOS, Proceedings of the 13 th ACM Great Lakes Symposium on VLSI April 2003, Pages: 15-20. DK Mohammad M. Mansour, Naresh R. Shanbhag, Session 11: Low-power VLSI decoder architectures for LDPC codes, Proceedings of the 2002 international symposium on Low power electronics and design August 2002, Pages: 284-289. DL R. Blahut, "Theory and Practice of Error Control Codes", Library of Congress Cataloging in Publication Data, pp-47-49, (May 1984) DM W. W. Peterson and E.J. Weldon, Jr., "Error-Correcting Codes", Second Edition, The			(same inventor) whole document.				
document. DC NN77112415. Digital Encoding of Wide Range Dynamic Analog Signals, IBM Tech. Disclosure Bulletin, November 1, 1997, VOL. No. 20; ISSUE No. 6; Pages 2415-2417, whole document DD NN9210335. Hierarchical Coded Modulation of Data with Fast Decaying Probability Distributions, IBM Tech. Disclosure Bulletin, October 1992, VOL. No. 35; ISSUE No. 5; Pages 335-336, whole document. DE Sorokine, V. et al. Innovative coding scheme for spread-spectrum communications, The Ninth IEEE International Symposium on Indoor and Mobile Radio Communications, pages: 1491-1495, Vol. 3; September 1998, whole document. DF T. Moors and M. Veeraraghavan, "Preliminary specification and explanation of Zing: An end-to-end protocol for transporting bulk data over optical circuits", pp. 1-55 (May 2001). DG T. Richardson and R. Urbanke, "The Capacity of Low-Density Parity-Check Codes under Message-Passing Decoding", pp. 1-44 (March 2001). DH T. Richardson, A. Shokrollahi, R. Urbanke, "Design of Capacity-Approaching Irregular Low-Density Parity-Check Codes", pp. 1-43 (March 2001). DI T. Richardson and R. Urbanke, "An Introduction to the Analysis of Iterative Coding Systems", pp. 1-36. DJ Saied Hemati, Amir H. Banihashemi, VLSI circuits: Iterative decoding in analog CMOS, Proceedings of the 13 th ACM Great Lakes Symposium on VLSI April 2003, Pages:15-20. DK Mohammad M. Mansour, Naresh R. Shanbhag, Session 11: Low-power VLSI decoder architectures for LDPC codes, Proceedings of the 2002 international symposium on Low power electronics and design August 2002, Pages: 284-289. DL R. Blahut, "Theory and Practice of Error Control Codes", Library of Congress Cataloging in Publication Data, pp.47-49, (May 1984) DM W. W. Peterson and E.J. Weldon, Jr., "Error-Correcting Codes", Second Edition, The		DB	Paranchych et al. Performance of a digital symbol synchronizer in cochannel interference				
DC NN77112415. Digital Encoding of Wide Range Dynamic Analog Signals, IBM Tech. Disclosure Bulletin, November 1, 1997, VOL. No. 20; ISSUE No. 6; Pages 2415-2417, whole document DD NN9210335. Hierarchical Coded Modulation of Data with Fast Decaying Probability Distributions, IBM Tech. Disclosure Bulletin, October 1992, VOL. No. 35; ISSUE No. 5; Pages 335-336, whole document. DE Sorokine, V. et al. Innovative coding scheme for spread-spectrum communications, The Ninth IEEE International Symposium on Indoor and Mobile Radio Communications, pages: 1491-1495, Vol. 3; September 1998, whole document. DF T. Moors and M. Veeraraghavan, "Preliminary specification and explanation of Zing: An end-to-end protocol for transporting bulk data over optical circuits", pp. 1-55 (May 2001). DG T. Richardson and R. Urbanke, "The Capacity of Low-Density Parity-Check Codes under Message-Passing Decoding", pp. 1-44 (March 2001). DH T. Richardson, A. Shokrollahi, R. Urbanke, "Design of Capacity-Approaching Irregular Low-Density Parity-Check Codes", pp. 1-43 (March 2001). DI T. Richardson and R. Urbanke, "An Introduction to the Analysis of Iterative Coding Systems", pp. 1-36. DJ Saied Hemati, Amir H. Banihashemi, VLSI circuits: Iterative decoding in analog CMOS, Proceedings of the 13 th ACM Great Lakes Symposium on VLSI April 2003, Pages: 15-20. DK Mohammad M. Mansour, Naresh R. Shanbhag, Session 11: Low-power VLSI decoder architectures for LDPC codes, Proceedings of the 2002 international symposium on Low power electronics and design August 2002, Pages: 284-289. DL R. Blahut, "Theory and Practice of Error Control Codes", Library of Congress Cataloging in Publication Data, pp.47-49, (May 1984) DM W. W. Peterson and E.J. Weldon, Jr., "Error-Correcting Codes", Second Edition, The			and noise, IEEE Transactions on Communications, pages: 1945-1954; Nov. 2000, whole				
Disclosure Bulletin, November 1, 1997, VOL. No. 20; ISSUE No. 6; Pages 2415-2417, whole document DD NN9210335. Hierarchical Coded Modulation of Data with Fast Decaying Probability Distributions, IBM Tech. Disclosure Bulletin, October 1992, VOL. No. 35; ISSUE No. 5; Pages 335-336, whole document. DE Sorokine, V. et al. Innovative coding scheme for spread-spectrum communications, The Ninth IEEE International Symposium on Indoor and Mobile Radio Communications, pages: 1491-1495, Vol. 3; September 1998, whole document. DF T. Moors and M. Veeraraghavan, "Preliminary specification and explanation of Zing: An end-to-end protocol for transporting bulk data over optical circuits", pp. 1-55 (May 2001). DG T. Richardson and R. Urbanke, "The Capacity of Low-Density Parity-Check Codes under Message-Passing Decoding", pp. 1-44 (March 2001). DH T. Richardson, A. Shokrollahi, R. Urbanke, "Design of Capacity-Approaching Irregular Low-Density Parity-Check Codes", pp. 1-43 (March 2001). DI T. Richardson and R. Urbanke, "An Introduction to the Analysis of Iterative Coding Systems", pp. 1-36. DJ Saied Hemati, Amir H. Banihashemi, VLSI circuits: Iterative decoding in analog CMOS, Proceedings of the 13th ACM Great Lakes Symposium on VLSI April 2003, Pages:15-20. DK Mohammad M. Mansour, Naresh R. Shanbhag, Session 11: Low-power VLSI decoder architectures for LDPC codes, Proceedings of the 2002 international symposium on Low power electronics and design August 2002, Pages: 284-289. DL R. Blahut, "Theory and Practice of Error Control Codes", Library of Congress Cataloging in Publication Data, pp-47-49, (May 1984) DM W. W. Peterson and E.J. Weldon, Jr., "Error-Correcting Codes", Second Edition, The							
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DD NN9210335. Hierarchical Coded Modulation of Data with Fast Decaying Probability Distributions, IBM Tech. Disclosure Bulletin, October 1992, VOL. No. 35; ISSUE No. 5; Pages 335-336, whole document. DE Sorokine, V. et al. Innovative coding scheme for spread-spectrum communications, The Ninth IEEE International Symposium on Indoor and Mobile Radio Communications, pages: 1491-1495, Vol. 3; September 1998, whole document. DF T. Moors and M. Veeraraghavan, "Preliminary specification and explanation of Zing: An end-to-end protocol for transporting bulk data over optical circuits", pp. 1-55 (May 2001). DG T. Richardson and R. Urbanke, "The Capacity of Low-Density Parity-Check Codes under Message-Passing Decoding", pp. 1-44 (March 2001). DH T. Richardson, A. Shokrollahi, R. Urbanke, "Design of Capacity-Approaching Irregular Low-Density Parity-Check Codes", pp. 1-43 (March 2001). DI T. Richardson and R. Urbanke, "An Introduction to the Analysis of Iterative Coding Systems", pp. 1-36. DJ Saied Hemati, Amir H. Banihashemi, VLSI circuits: Iterative decoding in analog CMOS, Proceedings of the 13 th ACM Great Lakes Symposium on VLSI April 2003, Pages: 15-20. DK Mohammad M. Mansour, Naresh R. Shanbhag, Session 11: Low-power VLSI decoder architectures for LDPC codes, Proceedings of the 2002 international symposium on Low power electronics and design August 2002, Pages: 284-289. DL R. Blahut, "Theory and Practice of Error Control Codes", Library of Congress Cataloging in Publication Data, pp-47-49, (May 1984) DM W. W. Peterson and E.J. Weldon, Jr., "Error-Correcting Codes", Second Edition, The							
Distributions, IBM Tech. Disclosure Bulletin, October 1992, VOL. No. 35; ISSUE No. 5; Pages 335-336, whole document. DE Sorokine, V. et al. Innovative coding scheme for spread-spectrum communications, The Ninth IEEE International Symposium on Indoor and Mobile Radio Communications, pages: 1491-1495, Vol. 3; September 1998, whole document. DF T. Moors and M. Veeraraghavan, "Preliminary specification and explanation of Zing: An end-to-end protocol for transporting bulk data over optical circuits", pp. 1-55 (May 2001). DG T. Richardson and R. Urbanke, "The Capacity of Low-Density Parity-Check Codes under Message-Passing Decoding", pp. 1-44 (March 2001). DH T. Richardson, A. Shokrollahi, R. Urbanke, "Design of Capacity-Approaching Irregular Low-Density Parity-Check Codes", pp. 1-43 (March 2001). DI T. Richardson and R. Urbanke, "An Introduction to the Analysis of Iterative Coding Systems", pp. 1-36. DJ Saied Hemati, Amir H. Banihashemi, VLSI circuits: Iterative decoding in analog CMOS, Proceedings of the 13th ACM Great Lakes Symposium on VLSI April 2003, Pages:15-20. DK Mohammad M. Mansour, Naresh R. Shanbhag, Session 11: Low-power VLSI decoder architectures for LDPC codes, Proceedings of the 2002 international symposium on Low power electronics and design August 2002, Pages: 284-289. DL R. Blahut, "Theory and Practice of Error Control Codes", Library of Congress Cataloging in Publication Data, pp-47-49, (May 1984) DM W. W. Peterson and E.J. Weldon, Jr., "Error-Correcting Codes", Second Edition, The				<u> </u>			
Pages 335-336, whole document. DE Sorokine, V. et al. Innovative coding scheme for spread-spectrum communications, The Ninth IEEE International Symposium on Indoor and Mobile Radio Communications, pages: 1491-1495, Vol. 3; September 1998, whole document. DF T. Moors and M. Veeraraghavan, "Preliminary specification and explanation of Zing: An end-to-end protocol for transporting bulk data over optical circuits", pp. 1-55 (May 2001). DG T. Richardson and R. Urbanke, "The Capacity of Low-Density Parity-Check Codes under Message-Passing Decoding", pp. 1-44 (March 2001). DH T. Richardson, A. Shokrollahi, R. Urbanke, "Design of Capacity-Approaching Irregular Low-Density Parity-Check Codes", pp. 1-43 (March 2001). DI T. Richardson and R. Urbanke, "An Introduction to the Analysis of Iterative Coding Systems", pp. 1-36. DJ Saied Hemati, Amir H. Banihashemi, VLSI circuits: Iterative decoding in analog CMOS, Proceedings of the 13 th ACM Great Lakes Symposium on VLSI April 2003, Pages:15-20. DK Mohammad M. Mansour, Naresh R. Shanbhag, Session 11: Low-power VLSI decoder architectures for LDPC codes, Proceedings of the 2002 international symposium on Low power electronics and design August 2002, Pages: 284-289. DL R. Blahut, "Theory and Practice of Error Control Codes", Library of Congress Cataloging in Publication Data, pp-47-49, (May 1984) DM W. W. Peterson and E.J. Weldon, Jr., "Error-Correcting Codes", Second Edition, The		DD					
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